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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/817,233	03/27/2001	Ryo Kubota	Q62494	8072

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SUGHRUE, MION, ZINN, MACPEAK & SEAS
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EXAMINER
LEE, HSIEN MING

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 06/28/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

'Offic Action Summary	Application No. 09/817,233	Applicant(s) KUBOTA ET AL.	
	Examiner Hsien-Ming Lee	Art Unit 2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-19 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-19 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5, 6 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Hsien Ming Lee
June 23, 2002

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 11 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In light of claim 2, the second gate electrode is formed in the second transistor, not in the first transistor. Thus, it not clear why claim 11, lines 2, 5 recites " first transistor."

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sung ('831) in view of applicants' admitted prior art ("AAPA").

Regarding claims 1-8, 10-11, 16-18, Sung teaches the claimed method of manufacturing a system-on-chip semiconductor device, including a CMOS logic circuit portion 50 and a DRAM portion 60, comprising :

- forming at least a first transistor on a substrate 1 at the CMOS logic circuit portion 50 (Fig. 10);
- forming at least a second transistor on a substrate 1 at the DRAM portion 60 (Fig. 10);
- forming an interlayer film 29 and 34 on the substrate 1 at the CMOS 50 and the DRAM portions 60, covering the at least a first transistor and the at least a second transistor (Fig. 18);
- forming a groove 36 in the interlayer film 29/34 by removing a portion of the interlayer film 29/34 at the DRAM portion 60 (Fig.18);
- forming a first polysilicon film 37 on an upper surface of the interlayer film 34/29 at the CMOS 50 and the DRAM 60 portions, and a second polysilicon film 37 on an inner wall of the groove 36 at the DRAM portion 60 (Fig. 18); and
- forming a first HSG on a surface of the first polysilicon film and a second HSG on a surface of the second polysilicon film (col. 7, lines 52-54).

Sung also teaches that forming the first and the second transistors include forming a first 7 (thickness : 40~60 Å) and a second gate insulating layer 8 (thickness : 50~70 Å) (Fig. 8; col. 4, lines 21-25); the second transistor comprises a peripheral circuit transistor and a switching transistor, wherein both transistor have similar structure ; wherein the step of forming the interlayer film 34/29 comprises the steps of forming a first silicon oxide 29 and a second silicon oxide 34 film; the method further comprising the steps of forming an opening in the first interlayer 29 over a diffusion region 31 of the switching transistor (Fig. 15); forming a capacitor electrode 33 in the opening in the first interlayer film 29 (Fig.17), wherein the capacitor

electrode 33 is connected to the diffusion region 31 of the switching transistor (Fig. 17); the groove 36 is formed in the second interlayer film 34 (Fig. 17) and the second polysilicon 37 is connected to the capacitor electrode 33 (Fig. 18); forming a capacitor film 38 on the first HSG film (not shown); and forming an upper electrode 39 on the capacitor film 38 (Fig. 19);

Regarding the last step of claim 1, Sung does not expressly teach removing the first HSG and the first polysilicon. However, it would have been obvious to one artisan in the art to appreciate that removing the first HSG and the first polysilicon on the upper surface of the interlayer film 34/29 and leaving the second HSG and the second polysilicon in the inner wall of the groove 36, prior to depositing a capacitor dielectric 38, is a necessary step during the manufacturing of a capacitor in the DRAM region 60.

Regarding claims 4, 12, 13 and 19, Sung does not teach forming a BPSG over the first interlayer film 29 as the second interlayer film 34. AAPA, however, teaches utilizing the BPSG as the second interlayer film 120 over the first interlayer film 116 (SiO2; Figs. 3C-3D) in the DRAM portion. Therefore, it would have been obvious to one artisan in the art at the time of the invention was made to replace the silicon oxide of Sung with the BPSG of AAPA as the second interlayer since by doing so it would provide a better planarization for the subsequent processing steps.

Regarding claim 9, Sung does not expressly teach the capacitor film 38 comprising Ta2O5 but does suggest that the film 38 can be an insulator with a high dielectric constant (col. 7, lines 55-57). AAPA, however, teaches utilizing the Ta2O5, which is a high-dielectric-constant material, as the capacitor film (page 2, lines 12-13) in the DRAM portion. Therefore, it would have been obvious to one artisan in the art at the time of the invention was made to

utilize the high-dielectric-constant material, as suggested by Sung, such as Ta2O2, as taught by AAPA, in the Sung's method of forming the capacitor in the DRAM region since by doing so it would improve the performance of the capacitor in the DRAM region.

Regarding claims 14 and 15, the selection of the surface area ratio of the memory cell portion is obvious because it is a matter of determining optimum process condition by routine experimentation for best results for the DRAM performance in conjunction with the consideration the size of CMOS logic circuit portion. In re Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious). In fact, AAPA teaches that the ration of memory cells 1 to the area of the chip 2 can be 50~60% (Fig. 6A; page 12, lines 14-16). In such situation, the applicants must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range. See M.P.E.P. 2144.05 III

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 703-305-7341. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-0142 for regular communications and 703-305-0142 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.